IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	Confirmation Number: 1520
John Christopher Rudin	Group Art Unit: 2814
Serial No.: 10/563,679	Examiner: Diana C. Garrity
Filed: June 9, 2006	Docket No.: 200300815-4

For: Thin Film Transistor Device With Metallic Electrodes

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Sir:

This Appeal Brief under 37 C.F.R. § 41.37 is submitted in support of the Notice of Appeal filed February 16, 2009, responding to the Final Office Action mailed December 29, 2008.

It is not believed that extensions of time or fees are required to consider this Appeal Brief. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required are hereby authorized to be charged to Deposit Account No. 08-2025.

I. Real Party in Interest

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. Related Appeals and Interferences

There are no known related appeals or interferences that will affect or be affected by a decision in this Appeal.

III. Status of Claims

Claims 1 – 9, 12, and 25 – 26 stand finally rejected. No claims have been allowed. Claims 13 – 18 and 21 – 22 have been withdrawn. Claims 10 – 11, 19 – 20 and 23 – 24 have been canceled. The final rejections of claims 1 – 9, 12, and 25 – 26 are appealed.

IV. Status of Amendments

No amendments have been made or requested since the mailing of the Final Office Action and all amendments submitted prior to the Final Office Action have been entered. The claims in the attached Claims Appendix reflect the present state of the pending claims.

V. Summary of Claimed Subject Matter

The claims are summarized below with reference numerals and references to the written description ("specification") and drawings. The subject matter described in the following appears in the original disclosure at least where indicated, and may further appear in other places within the original disclosure.

Embodiments according to independent claim 1 describe a transistor device having a metallic source electrode (page 8, line 26 and FIG. 2, element S), a metallic drain electrode (page 8, line 26 and FIG. 2, element D), a metallic gate electrode (page 8, line 26 and FIG. 2, element G) and a channel (page 8, line 7 and FIG. 1E, element 326) in a deposited semiconductor material (page 7, line 26 and FIG. 1F, element 330), the transistor device comprising: a first layer (page 8, line 28 and FIG. 1G, element 316) comprising the metallic gate electrode (page 8, line 26 and FIG. 2, element G), a first metal portion of the metallic source electrode (page 8, line 28 and FIG. 1H, element 310c) and a first metal portion of the metallic drain electrode (page 8, line 26 and FIG. 1H, element 324a); a second layer (page 8, line 30 and FIG. 1G, element 318) comprising a second metal portion of the metallic source electrode (page 8, line 28 and FIG. 1H, element 324c), a second metal portion of the metallic drain electrode (page 8, line 28 and FIG. 1H, element 324a), the deposited semiconductor material (page 7, line 26 and FIG. 1F, element 330) and dielectric material (FIG. 1E, element 322 and page 8, line 32) between the semiconductor material (page 7, line 26 and FIG. 1F, element 330) and the metallic gate electrode (page 8, line 26 and FIG. 2, element G); and a third layer (page 9, line 1 and FIG. 1G, element 320) comprising a substrate (page 9, line 1 and FIG. 1G, element 314), wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer (page 9, line 1 and FIG. 2).

Embodiments according to independent claim 25 describe a transistor device having a metallic source electrode (page 8, line 26 and FIG. 2, element S), a metallic drain electrode (page 8, line 26 and FIG. 2, element D), a metallic gate electrode (page 8, line 26 and FIG. 2, element G) and a channel (page 8, line 7 and FIG. 1E, element 326) in a deposited semiconductor material (page 7, line 26 and FIG. 1F, element 330), the transistor device comprising: a first upper planar layer (page 8, line 28 and FIG. 1G, element 316) comprising the metallic gate electrode (page 8, line 26 and FIG. 2, element G), a first metal portion of the metallic source electrode (page 8, line 28 and FIG. 1H, element 310c) and a first metal portion of the metallic drain electrode (page 8, line 26 and FIG. 1H, element 324a); a second middle planar layer (page 8, line 30 and FIG. 1G, element 318) comprising a second metal portion of the metallic source electrode (page 8, line 28 and FIG. 1H, element 324a), a second metal portion of the metallic drain electrode (page 8, line 28 and FIG. 1H, element 324a), the deposited semiconductor material (page 7, line 26 and FIG. 1F, element 330) and dielectric material (FIG. 1E, element 322 and page 8, line 32) between the semiconductor material (page 7, line 26 and FIG. 1F, element 330) and the metallic gate electrode (page 8, line 26 and FIG. 2, element G); and a third lower planar layer (page 9, line 1 and FIG. 1G, element 320) comprising a substrate (page 9, line 1 and FIG. 1G, element 314), wherein first, second and third planar layers are arranged in order such that the second middle layer (page 8, line 30 and FIG. 1G, element 318) is positioned between the first upper layer (page 8, line 28 and FIG. 1G, element 316) and the third lower layer (page 9, line 1 and FIG. 1G, element 320), wherein the metallic source electrode (page 8, line 26 and FIG. 2, element S), drain electrode (page 8, line 26 and FIG. 2, element D) and gate electrode (page 8, line 26 and FIG. 2, element G) comprise electro-deposited metal, the gate electrode (page 8, line 26 and FIG. 2, element G) occupies only the first upper planar layer(page 8, line 28 and FIG. 1G, element 316) and the channel (page 8, line 7 and FIG. 1E,

element 326) occupies only the second middle planar layer (page 8, line 30 and FIG. 1G, element 318), the metallic source electrode (page 8, line 26 and FIG. 2, element S) consists of the first metal portion of the metallic source electrode (page 8, line 28 and FIG. 1H, element 310c) overlying the second metal portion of the metallic source electrode (page 8, line 28 and FIG. 1H, element 324a) and the metallic drain electrode (page 8, line 26 and FIG. 2, element D) consists of the first metal portion of the metallic drain electrode (page 8, line 28 and FIG. 1H, element 324a) overlying the second metal portion of the metallic drain electrode (page 8, line 26 and FIG. 2, element D).

VI. Grounds of Rejection to be Reviewed on Appeal

The following grounds of rejections are to be reviewed on appeal:

Claims 1 – 9 and 25 – 26 stand rejected under 35 U.S.C. §102 for allegedly being for allegedly being unpatentable over *Shi* (U.S. Patent Number 6,326,640).

Claim 12 stands rejected under 35 U.S.C. §103 for allegedly being unpatentable over *Shi* (U.S. Patent Number 6,326,640).

VII. Arguments

Appellant respectfully submits that Appellant's claims 1 – 9 and 25 – 26 are patentable under 35 U.S.C. §102 and claim 12 is patentable under 35 U.S.C. §103. Appellant respectfully requests that the Board of Patent Appeals overturn the final rejection of those claims at least for the reasons discussed below.

A. The *Shi* Reference

Shi discloses an "organic thin film transistor including a gate on a layer of gate insulator material, a source and a drain positioned in spaced apart relationship on a film of organic semiconductor material with uniaxially aligned molecules" (Abstract).

B. Rejections Under 35 U.S.C. §102

1. Claim 1 is Allowable Over *Shi*

The Final Office Action indicates that claim 1 stands rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Number 6,326,640 ("*Shi*"). Appellant respectfully traverses this rejection on the grounds that *Shi* does not disclose, teach, or suggest all of the claimed elements. More specifically, claim 1 recites:

> A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:
>
> a first layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;
>
> ***a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode***, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and
>
> a third layer comprising a substrate, wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer.

(Emphasis added).

Appellant respectfully submits that claim 1 is allowable over the cited art for at least the reason that *Shi* fails to disclose, teach, or suggest a "transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising… ***a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode***, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode" as recited in claim 1. More specifically, the Final Office Action argues that "***a second layer comprising a second metal portion of the metallic source***

electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode" of claim 1 is "a product by process limitation and is given no patentable weight" (OA page 3, line 1). Appellant disagrees. Nowhere in claim 1 is there any indication of a process whatsoever. This element of claim 1 merely recites the elements of the second layer. No process is even suggested in this element or elsewhere in claim 1. For at least this reason, this rejection is improper and should be withdrawn.

Further, the Final Office Action argues that because this element of claim 1 is allegedly a product by process element, the Final Office Action is justified in arbitrarily dividing the electrode. More specifically, the Final Office Action argues the "upper half" of 75 as the first metal portion of the metallic source electrode and the "lower half" of element 75 as the second metal portion of the metallic source electrode (with similar analysis for element 76) (OA page 5, first and second paragraphs). However, this is an incorrect inference. Referring to FIG. 7 of *Shi*, the conductive strips 75 and 76 are single piece elements and thus are part of only one layer. Consequently, the Final Office Action's arbitrary division of these elements into an "upper half" and a "lower half" is impermissible under the requirements of 35 U.S.C. §102. Further nowhere does *Shi* even suggest "***a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode***" as recited in claim 1. For at least this reason, claim 1 is allowable.

2. **Claim 25 is Allowable Over *Shi***

The Final Office Action indicates that claim 25 stands rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Number 6,326,640 ("*Shi*"). Appellant respectfully traverses this rejection on the grounds that *Shi* does not disclose, teach, or suggest all of the claimed elements. More specifically, claim 25 recites:

> A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:
>
> a first upper planar layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;
>
> ***a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode***, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and
>
> a third lower planar layer comprising a substrate, wherein first, second and third planar layers are arranged in order such that the second middle layer is positioned between the first upper layer and the third lower layer,
>
> wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal, the gate electrode occupies only the first upper planar layer and the channel occupies only the second middle planar layer, the metallic source electrode consists of the first metal portion of the metallic source electrode overlying the second metal portion of the metallic source electrode and the metallic drain electrode consists of the first metal portion of the metallic drain electrode overlying the second metal portion of the metallic drain electrode.

(Emphasis added).

Appellant respectfully submits that claim 25 is allowable over the cited art for at least the reason that *Shi* fails to disclose, teach, or suggest a "transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising … ***a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode***, the

deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode" as recited in claim 25. More specifically, the Final Office Action argues that "***a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode***" of claim 25 is "a product by process limitation and is given no patentable weight" (OA page 3, line 1). Appellant disagrees. Nowhere in claim 25 is there any indication of a process whatsoever. This element of claim 25 merely recites the elements of the second layer. No process is even suggested in this element or elsewhere in claim 1. For at least this reason, this rejection is improper and should be withdrawn.

Further, the Final Office Action argues that because this element of claim 25 is allegedly a product by process element, the Final Office Action is justified in arbitrarily dividing the electrode. More specifically, the Final Office Action argues the "upper half" of 75 as the first metal portion of the metallic source electrode and the "lower half" of element 75 as the second metal portion of the metallic source electrode (with similar analysis for element 76) (OA page 5, first and second paragraphs). However, this is an incorrect inference. Referring to FIG. 7 of *Shi*, the conductive strips 75 and 76 are single piece elements and thus are part of only one layer. Consequently, the Final Office Action's arbitrary division of these elements into an "upper half" and a "lower half" is impermissible under the requirements of 35 U.S.C. §102. Further nowhere does *Shi* even suggest "***a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode***" as recited in claim 25. For at least this reason, claim 25 is allowable.

3. Claims 2 – 9 and 26 are Allowable Over *Shi*

The Final Office Action indicates that claims 2 – 9 and 26 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Number 6,326,640 ("*Shi*"). Appellant respectfully traverses this rejection on the grounds that *Shi* does not disclose, teach, or suggest all of the claimed elements. More specifically, dependent claims 2 – 9 and 26 are believed to be allowable for at least the reason that these claims depend from and include the elements of allowable independent claim 1. *In re Fine*, *Minnesota Mining and Mfg.Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir. 2002).

C. Rejections Under 35 U.S.C. §103 – Claim 12 is Allowable Over *Shi*

The Office Action indicates that claim 12 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 6,326,640 ("*Shi*"). Appellant respectfully traverses this rejection for at least the reason that *Shi* fails to disclose, teach, or suggest all of the elements of claim 12. More specifically, dependent claim 12 is believed to be allowable for at least the reason that this claim depends from and include the elements of allowable independent claim 1. *In re Fine*, *Minnesota Mining and Mfg.Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir. 2002).

VIII. Conclusion

In summary, the pending claims are patentable over the applied cited art references and that the rejection of these claims should be withdrawn. Appellant therefore respectfully requests that the Board of Appeals overturn the Examiner's rejection and allow the pending claims.

Respectfully submitted,

By: _____/afb/_____
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Claims Appendix under 37 C.F.R. § 41.37(c)(1)(viii)

The following are the claims that are involved in this Appeal.

1. A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:

a first layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;

a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and

a third layer comprising a substrate, wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer.

2. A transistor device as claimed in claim 1, wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal.

3. A transistor device as claimed in claim 1, wherein the first, second and third layers are each of respective substantially uniform thickness.

4. A transistor device as claimed in claim 1, wherein the third layer includes adhesive bonding the substrate to the transistor device.

5. A transistor device as claimed in claim 1, wherein the first layer has a substantially planar surface comprising substantially planar portions of the source, drain and gate electrodes.

6. A transistor device as claimed in claim 1, wherein the deposited semiconductor material comprises organic semiconductor material.

7. A transistor device as claimed in claim 1, wherein the deposited semiconductor material comprises indications that it was deposited from liquid.

8. A transistor device as claimed in claim 1, wherein the semiconductor material is embedded in the device and overlain by the gate electrode.

9. A transistor device as claimed in claim 1 further comprising insulating material separating the gate electrode from the source electrode and the drain electrode.

12. A substrate for a display device comprising a plurality of transistor devices as claimed in claim 1.

25. A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:

a first upper planar layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;

a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and

a third lower planar layer comprising a substrate, wherein first, second and third planar layers are arranged in order such that the second middle layer is positioned between the first upper layer and the third lower layer,

wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal, the gate electrode occupies only the first upper planar layer and the channel occupies only the second middle planar layer, the metallic source electrode consists of the first metal portion of the metallic source electrode overlying the second metal portion of the metallic source electrode and the metallic drain electrode consists of the first metal portion of the metallic drain electrode overlying the second metal portion of the metallic drain electrode.

26. A transistor device as claimed in claim 1, wherein the metallic source, gate and drain electrodes consist entirely of electro-deposited material and the metallic gate electrode contacts the dielectric material.

Evidence Appendix under 37 C.F.R. § 41.37(c)(1)(ix)

(None)

Related Proceedings Appendix under 37 C.F.R. § 41.37(c)(1)(x)

(None)